REMARKS

Claims 7-12 stand rejected under 35 USC §101 as being directed to non-statutory subject matter. Claims 1-18 stand rejected under 35 USC §102(b) as being anticipated by Yuan et al., U.S. patent 6,321,186.

Claims 1, 7, and 13 have been amended to more clearly state the invention and in an earnest attempt to clearly distinguish the invention from the prior art references of record.

Claim 7 has been amended to accommodate the Examiner's rejection under 35 USC §101. As amended, claim 7 recites that the computer program product including instructions stored on a computer recording medium, wherein said instructions, when executed by the computer system cause the computer system to perform the steps of. Thus, independent claim 7, as amended, is believed to clearly recite statutory subject matter. Reconsideration and withdrawal of the rejection of claims 7-12 under 35 USC §101 is respectfully requested.

Reconsideration and allowance of the pending claims 1-18, as amended, is respectfully requested.

Yuan et al., U.S. patent 6,321,186 discloses a method for verifying an integrated circuit design using constraint information to develop a weighted data structure. In one embodiment, a binary decision diagram (BDD) includes a plurality of nodes (401, 402, 403, 404, 405, 406, 407, 420, and 430) representing signals and states in the circuit, and each node has a branching probability based on user-defined weights. The BDD represents the intersection of the input space and state space which

satisfies the constraints. Current state information resulting from simulation is used to dynamically adjust the branching probabilities of the BDD on the fly. In one embodiment, the constraint information is applicable for formal verification of a portion of the circuit. In another embodiment, a simulation controller (12) receives design and constraint information and generates the program to control simulator (14). Column 2, lines 29-37 states:

A simulation controller provides a set of simulation inputs to a simulator, where the simulation inputs are based on the logic data structure and the probabilities that a node will be in a given state. The simulation controller receives present state information from the simulator, and adjusts the weights and probabilities of the BDD accordingly. The state information is then dynamically incorporated into the BDD.

Column 7, lines 10-18 states:

State information can be considered in the computation of branching probabilities by defining the probability of assigning an input to 1 as a function of state variables. Such a definition can be introduced by the user by providing an expression, for example in Verilog or VHDL. Such an expression may involve any state variables of the design. The expression evaluates to a number between 0 and 1 when state variables assume specific values depending upon the current state of the design.

Column 9, line 63 through column 10, line13 states:

Generation of the simulation inputs depends upon an actual calculation of the likelihood of the true branch being taken based upon the node weights calculated in step 234. Simulation controller 12 generates simulation inputs appropriate to the present state, and the branching probabilities that will be discussed in the next paragraph. Once the simulation controller 12 has settled on a stable model, simulator 14 simulates the design using that model. After this simulation, the present state of the circuit is sampled and the process continues as before. A user-determined stop criteria, such as a maximum time or a maximum number of cycles, or a false final result will stop the process. At each clock cycle, the outcome of simulation either results in an input that satisfies the constraints or results in no valid inputs for the current state. If there are no valid inputs the program aborts. This typically can occur when there are some constraints involving only state variables or if the user-defined weights eliminated all possible successful paths.

Applicants respectfully submit that each of the independent claims 1, 7, and 13, as amended, is patentable over the references of record including Yuan et al. Independent claims 1, 7, and 13, as amended, recite a method, a computer program product, and apparatus for implementing a level bias function, or an operand level bias, for branch prediction control for generating test simulation vectors. In the present invention, as illustrated and described in the specification, a level bias function function134 enables reliably predicting whether or not a branch will be taken, in all test cases, and the need to rely on any hard coded values as used in the past is eliminated.

Independent claim 1 recites method steps for implementing a level bias function for branch prediction control for generating test simulation vectors that are not disclosed, nor suggested by Yuan et al. More specifically, the recited steps of "providing a universal set of values for a branch operand field BO; and reducing said universal set for said branch operand field BO to include a set of valid values using said current resource values and based upon said user selected constraints; said branch operand field defining conditions under which a branch is taken for said branch conditional instruction" are not disclosed, nor suggested by Yuan et al.

Anticipation is a question of fact. In re King, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986). The inquiry as to whether a reference anticipates a claim must focus on what subject matter is encompassed by the claim and what subject matter is described by the reference. As set forth by the court in Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 218 USPQ 781, 789 (Fed. Cir. 1983), cert. denied, 465 U.S. 1026

(1984), it is only necessary for the claims to "'read on' something disclosed in the reference, i.e., all limitations in the claim are found in the reference, or 'fully met' by it." Anticipation under § 102 can be found only when the reference discloses exactly what is claimed; where there are differences between the reference disclosure and the claim, the rejection must be based on § 103 which takes differences into account. Tyler Refrigeration v. Kysor Industrial Corp., 777 F.2d 687, 689, 227 U.S.P.Q. 845 846-47 (Fed. Cir. 1985). It must be shown that the reference contains all of the elements of the claims, and that the elements are arranged in the same way to achieve the same result which is asserted to be an inventive function.

The Yuan et al. patent does not disclose, nor suggest the step of providing a universal set of values for a branch operand field BO, as taught by Applicants and claimed in independent claim 1, as amended. The Yuan et al. patent does not disclose, nor suggest the step of reducing said universal set for said branch operand field BO to include a set of valid values using said current resource values and based upon said user selected constraints; said branch operand field defining conditions under which a branch is taken for said branch conditional instruction, as taught by Applicants and claimed in independent claim 1, as amended. Thus, independent claim 1, as amended, is not anticipated by and is patentable over Yuan et al.

Lack of novelty can be established only where a prior invention is identical to (or "anticipates") the invention sought to be patented. "In addition, the prior art reference must be enabling, thus placing the allegedly disclosed matter in the

possession of the public." Akzo N.V. v. U.S. Intern. Trade Com'n, 808 F.2d 1471, 1479 (Fed. Cir. 1986). Thus, independent claim 1, as amended, is patentable.

Independent claim 7 recites a computer program product for implementing a level bias function for branch prediction control for generating test simulation vectors including steps that are not disclosed, nor suggested by Yuan et al. More specifically, the recited steps of "providing a universal set of values for a branch operand field BO; and reducing said universal set for said branch operand field BO to include a set of valid values using said current resource values and based upon said user selected constraints; said branch operand field defining conditions under which a branch is taken for said branch conditional instruction" are not disclosed, nor suggested by Yuan et al.

Thus, independent claim 7, as amended, is patentable for the same reasons as set forth above with respect to independent claim 1, as amended.

Independent claim 13, as amended, recites apparatus for implementing an operand level bias for branch prediction control for generating test simulation vectors. As amended, independent claim 7 recites a level bias function for providing a universal set of values for a branch operand field BO of said branch condition register (CR) and for reducing said universal set for branch operand field BO to include a set of valid values using said current resource values and based upon said user selected constraints; said branch operand field BO defining conditions under which a branch is taken for said branch conditional instruction.

The Yuan et al. patent does not disclose, nor suggest the recited level bias function, as taught and claimed by Applicants, as expressly recited in independent

claim 13, as amended.

Thus, independent claim 13, as amended, is patentable.

The Yuan et al. patent teaches the use of a logic data structure or binary decision diagram (BDD) to represent a circuit functionally, and teaches using a method for verifying a design of an integrated circuit having a set of functional constraints first generates a logic data structure based on the set of functional constraints, where the logic data structure comprises a plurality of nodes representing functional signals and each of the input signals has a predetermined weight. A node weight is then computed for each of the plurality of nodes based on the predetermined input weight. The method continues by generating a first set of simulation inputs based on the logic data structure and probabilities, and then simulating the integrated circuit design using the first set of simulation inputs to initialize the circuit's state. Applicants respectfully submit that the teachings and methods of the Yuan et al. patent are different from and do not anticipate, nor render obvious the claimed invention, as recited in independent claims 1, 7, and 13, as amended.

Dependent claims 2-6, 8-12, and 14-18 further define the invention of patentable claims 1, 7, and 13, and are likewise patentable.

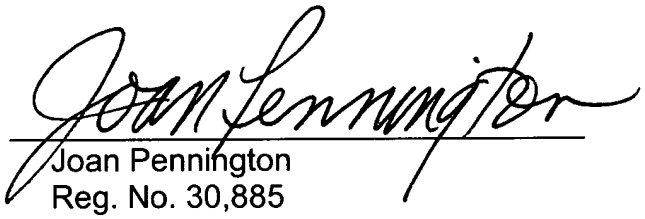
Applicants have reviewed all the art of record, and respectfully submit that the claimed invention is patentable over all the art of record, including the references not relied upon by the Examiner for the rejection of the pending claims.

It is believed that the present application is now in condition for allowance and allowance of each of the pending claims 1-18, as amended, is respectfully

requested. Prompt and favorable reconsideration is respectfully requested.

If the Examiner upon considering this amendment should find that a telephone interview would be helpful in expediting allowance of the present application, the Examiner is respectfully urged to call the applicants' attorney at the number listed below.

Respectfully submitted,

By: 

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